Appeal No. 16-2219

United States Court of Appeals for the Federal Circuit

PLL TECHNOLOGIES, INC.,
Appellant,

v.

XILINX, INC.,
Appellee.

Appeal from the United States Patent and Trademark Office,
Patent Trial and Appeal Board in IPR2015-00148

BRIEF OF APPELLEE XILINX, INC.

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CERTIFICATE OF INTEREST

Pursuant to Federal Circuit Rule 47.4, undersigned counsel for Appellee Xilinx, Inc., certifies the following:

1. The full name of every party or amicus represented by me is:

Xilinx, Inc.

2. The names of the real parties in interest, if different from the parties named above, are:

N/A

3. The names of all parent corporations and any publicly held companies that own 10% or more of the stock of the party represented by me are:

N/A

4. The names of all law firms and the partners and associates that appeared for Appellee in the trial court or agency or are expected to appear in this court are:

JONES DAY: Gregory A. Castanias; David B. Cochran; Joseph M. Sauer; Patrick T. Michael, Matthew J. Silveira; Joshua R. Nightingale

Dated: December 5, 2016

/s/ Matthew J. Silveira
Attorney for Appellee Xilinx, Inc.

TABLE OF CONTENTS

Page

TABLE OF CONTENTS
(continued)

Page

TABLE OF CONTENTS
(continued)

Page

TABLE OF AUTHORITIES

Page

CASES

STATUTES

OTHER AUTHORITIES

TABLE OF ABBREVIATIONS

Parties

Xilinx	Appellee Xilinx, Inc., the Petitioner in IPR2015-00148
PLL	Appellant PLL Technologies, Inc., the owner of the patent-at-issue
PTAB or the Board	The Patent Trial and Appeal Board of the United States Patent and Trademark Office

Cites

Appx__	Joint Appendix at page(s) __
BlueBr.	PLL's Opening Brief, Dkt. No. 21

Terms

'122 Patent	U.S. Patent No. 6,356,122, entitled "Clock Synthesizer with Programmable Input-Output Phase Relationship," and issued on March 12, 2002
PTO	The United States Patent and Trademark Office
AIA	The America Invents Act
APA	The Administrative Procedures Act

**All emphasis added unless otherwise indicated*

STATEMENT OF RELATED CASES

Pursuant to Federal Circuit Rule 47.5, counsel for Appellant Xilinx, Inc., provides as follows:

1. There has been no previous appeal in this case.

2. Although counsel is aware of no cases pending before this Court that may directly affect the Court's decision in this appeal, PLL has sued Xilinx for infringement of the '122 patent in the United States District Court for the District of Delaware. *See PLL Technologies, Inc. v. Xilinx, Inc.*, No. 14-945 (LPS) (CJB) (D. Del.). That case has been stayed pending resolution of this *inter partes* review proceeding, including all appeals.

INTRODUCTION

The '122 patent is directed to a clock synthesizer based on a phase-locked loop. After PLL sued Xilinx for infringement, Xilinx petitioned for *inter partes* review of the '122 patent. The Board instituted trial to review the patentability of claims 1-10, 12-14, and 16-20 based on two primary references—Nienaber and Young—and subsequently found all instituted claims to be obvious. PLL's appeal of that decision rests on two main arguments: (1) that the Board's obviousness analysis was premised on erroneous factual findings; and (2) that the *inter partes* review process is inherently unfair to patent owners. Both arguments lack merit.

First, PLL challenges the Board's claim constructions and its finding that the person of ordinary skill in the art (POSITA) would be motivated to combine Nienaber and Young. Although the Board's constructions of the terms "clock" and "programmable delay circuit" are dictated by the language of the claims and the specification—neither of which limits a clock to a digital system or requires a memory for a programmable delay circuit—PLL relied heavily on extrinsic evidence to support the contrary constructions it proposed. The Board's findings based on that extrinsic evidence are supported by substantial evidence, and PLL does not dispute that Nienaber discloses a clock and Young discloses a programmable delay circuit under the Board's constructions. Substantial evidence

also supports the Board's findings on the quintessentially factual issue of the POSITA's motivation to combine Nienaber and Young.

Second, lacking a case on the merits, PLL tries to manufacture a procedural error, arguing that the Board violated the APA and complaining generally about a patent owner's "severely constrained" ability to amend claims in *inter partes* review and similar proceedings created by the AIA. (BlueBr. 37.) But the Board followed the procedures mandated by the AIA and its implementing regulations to the letter. PLL's complaints are properly directed to Congress and the PTO, not this Court. Ironically, PLL failed to take advantage of many of the procedural mechanisms provided by the PTO to address the concerns it now raises on appeal (including by not moving to amend its claims), while other of its complaints are contradicted by the record. PLL's dissatisfaction with the *inter partes* review process is not a basis to second-guess the Board's reasoned decision and factual findings following a full and fair trial.

For these and the reasons stated more fully below, the Court should affirm.

JURISDICTIONAL STATEMENT

Xilinx agrees with PLL's jurisdictional statement. (BlueBr. 1.)

STATEMENT OF THE ISSUES

1. Whether the Board's finding that Nienaber discloses a "clock" is supported by substantial evidence where (i) the Board correctly construed that term

based on the intrinsic and extrinsic evidence, (ii) PLL does not dispute that Nienaber discloses a clock under the Board's construction, and (iii) the Board correctly found that Nienaber discloses a clock even under PLL's proposed construction.

2. Whether the Board's finding that Young discloses a "programmable delay circuit" is supported by substantial evidence where (i) the Board correctly construed that term based on the intrinsic and extrinsic evidence, and (ii) PLL does not dispute that Young discloses a programmable delay circuit under the Board's construction.

3. Whether substantial evidence supports the Board's finding that the POSITA would have been motivated to combine Nienaber and Young where the Board (i) provided articulated reasoning with rational underpinning as to why the POSITA would have combined the references, and (ii) rejected PLL's arguments that relied on an erroneous "bodily incorporation" test of obviousness.

4. Whether PLL can establish an APA violation despite having had multiple opportunities to respond to the evidence and arguments in Xilinx's Reply.

5. Whether PLL can establish that the Board's Final Written Decision violated the APA by relying on purportedly "new rationales" despite PLL having had notice of the alleged new rationales and an opportunity to address them.

STATEMENT OF THE CASE

A. The '122 Patent

The '122 patent relates to a phase-locked-loop-based clock synthesizer that generates output frequencies based on a reference clock input. (Appx48 at 1:10-15.) Figure 1 of the patent, which is included as background information, shows a conventional phase-locked loop having (i) a reference path for providing REF CLOCK (a reference signal) to a first input of a Phase Frequency Detector, and (ii) a feedback path for providing a feedback signal from a voltage-controlled oscillator (VCO) to a second input of the Phase Frequency Detector (*id.* at 1:19-42):

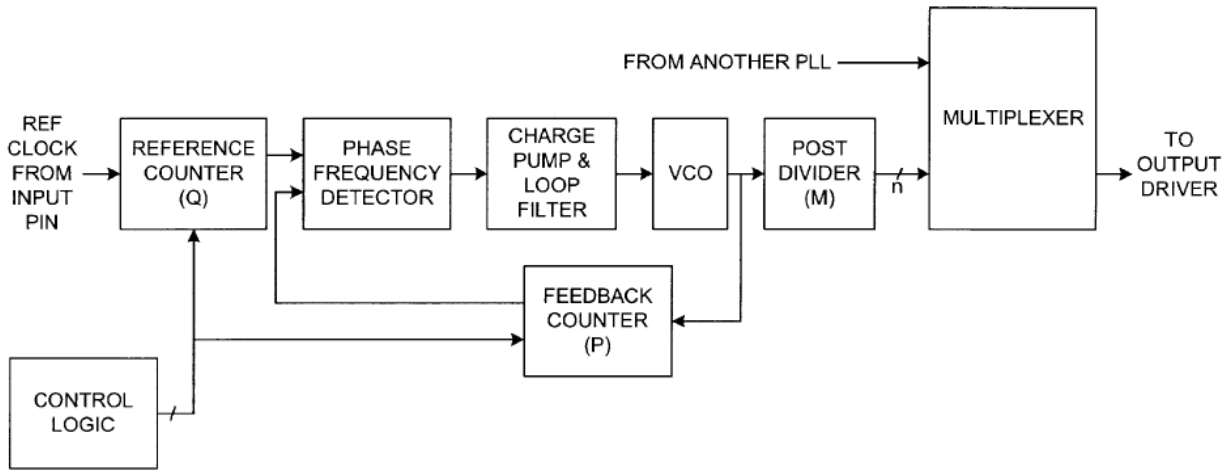


FIG. 1
(CONVENTIONAL)

(Appx46.)

Figure 2 is the only illustrated embodiment of the alleged invention of the '122 patent. This figure illustrates a "Conventional PLL" (shown within the

dotted lines) with the addition of a Programmable Delay DL2 and a Feedback Control Switch on the feedback path:

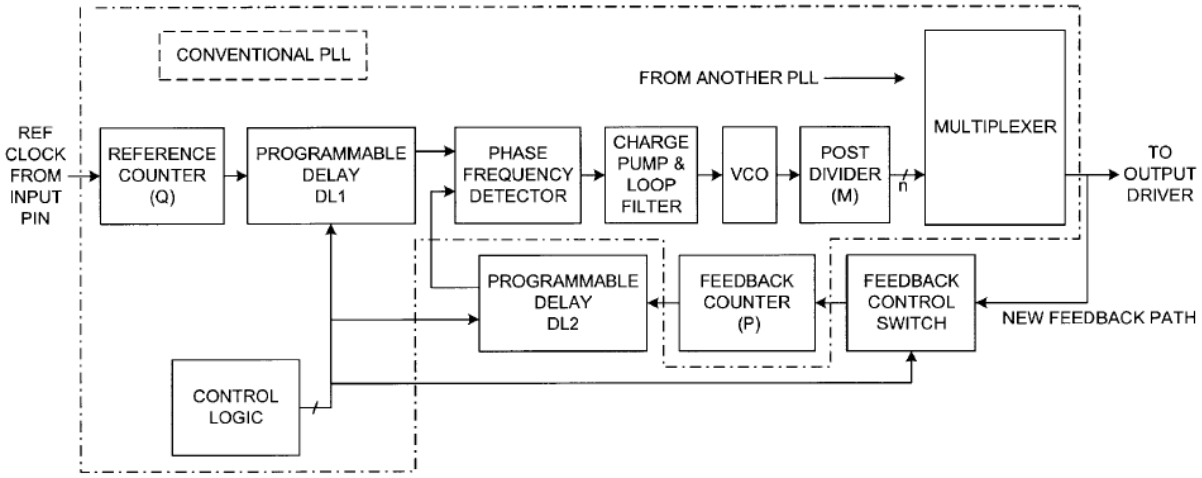


FIG. 2

(Appx47.)

Because there is also a programmable delay (Programmable Delay DL1) on the reference path in the "Conventional PLL" portion of Figure 2, the '122 patent teaches that programmable delay circuits were known in the art. In fact, the '122 patent states that "[i]n the present invention, the programmable delay circuit may be *conventional*." (Appx49 at 3:40-41.) Thus, the '122 patent was at most asserting that the *placement* of a programmable delay circuit on the feedback path was new, a fact made clear by the prosecution history.

During prosecution of the '122 patent, Applicants submitted original claims that only required "*at least one* of the reference path and the feedback path …

comprises a programmable delay circuit." (Appx458.) The Examiner rejected certain of the original claims as being anticipated by Young (U.S. Pat. No. 5,446,867), the same reference subsequently applied in the IPR proceeding that is the subject of this appeal. (Appx469.) The Examiner found that Young discloses a programmable delay circuit in the feedback path, as well as the other limitations recited in the rejected claims. (*Id.*)

In response, Applicants did not dispute that Young teaches a programmable delay circuit but instead amended the claims to require "*each of* the reference path and the feedback path … comprises a programmable delay circuit." (Appx475-477.) The Examiner allowed the amended claims because he thought that the closest prior art of record failed to disclose a circuit that includes programmable delay circuits in *each of* the reference path and the feedback path. (Appx519-521.)

Independent claim 1, as issued, is reproduced below as a representative example of the allowed claims. The italicized text below shows the only portion of the claim that is not part of the "Conventional PLL" shown in Figure 2 of the '122 patent:

> 1. A clock circuit, comprising:
>
> an oscillator, having a reference input receiving a reference signal, a feedback input receiving a feedback signal, and an output;
>
> a reference path providing said reference signal from a reference clock input; and

> a feedback path providing said feedback signal from the oscillator output;
>
> wherein each of the reference path *and the feedback path* comprises a programmable delay circuit.

(Appx50 at 5:25-35.)

B. The Cited References

1. Nienaber

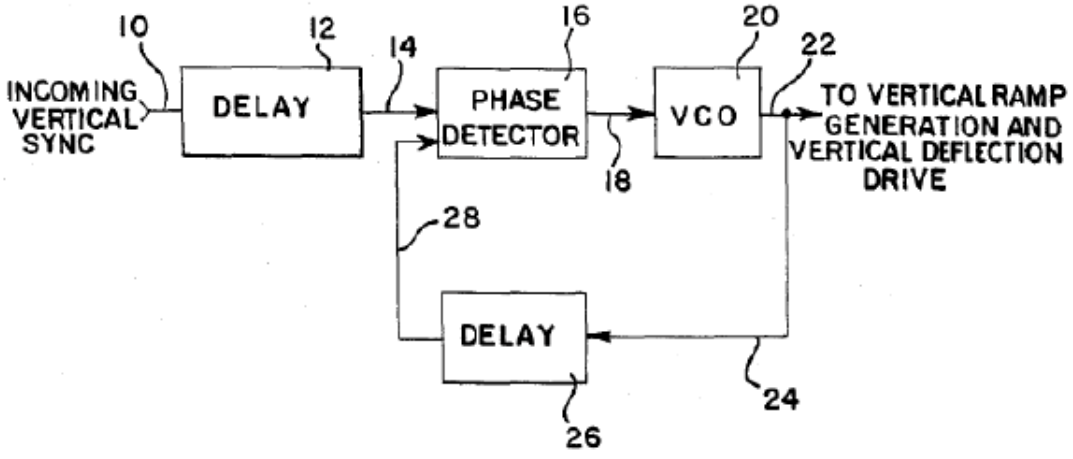
U.S. Patent No. 4,611,230 ("Nienaber"), entitled "Vertical Video Centering Control System," is directed to improvements in the television and video display arts. (Appx522-526.) When Nienaber was filed, video signals were "displayed on a raster display with progressive horizontal line scanning in which successive horizontal lines of video are written on the screen from left to right, top to bottom." (Appx524 at 1:11-14.) To return the scanning electron beam from the display's bottom right to its top left, a vertical synchronization signal was used: "[T]he horizontal line scanning is discontinued at some point in the lower right hand corner of the display screen and initiated in the upper left hand corner in response to the recognition of a vertical synchronization (sync) signal." (*Id.* at 1:17-21.)

In televisions and computer monitors at the time of Nienaber, a vertical position of the video on the display screen depended on the time at which the vertical sync signal was asserted. (*Id.* at 1:22-26.) For example, Nienaber describes that by delaying the assertion of the vertical sync signal "for

approximately the duration for one vertical field interval," the video may be moved both up and down on the display raster. (*Id.* at 2:3-11.) Nienaber describes, however, that "undesirable effects may frequently be encountered" when shifting the video up and down using then conventional procedures. (*Id.* at 2:11-14.) These undesirable effects include "side effects on product safety, picture linearity, video bandwidth or video definition." (*Id.* at 2:24-25.)

After describing the deficiencies of the conventional solutions, Nienaber discloses a new circuit for shifting a video display in both up and down directions "without creating undesirable side effects." (*Id.* at 2:55-58.) To enable a "video display [to] be desirably shifted in either vertical direction" (Appx525 at 3:61-62), Nienaber discloses a phase-locked loop circuit with (i) an adjustable delay circuit 12 in the reference path, and (ii) an adjustable delay circuit 26 in the feedback path. (*Id.* at 3:46-48.) This circuit is illustrated in Figure 1 of Nienaber:

FIG. 1



(Appx523.) "[B]y adjusting one or both of the delay values for the delay circuits 12 and 26, the video display may be desirably shifted in either vertical direction." (Appx525 at 3:60-62.)

2. Young

U.S. Patent No. 5,446,867 ("Young") is entitled "Microprocessor PLL Clock Circuit With Selectable Delayed Feedback." (Appx527-535.) Young discloses a phase-locked loop circuit having a delay line 27 in the feedback path:

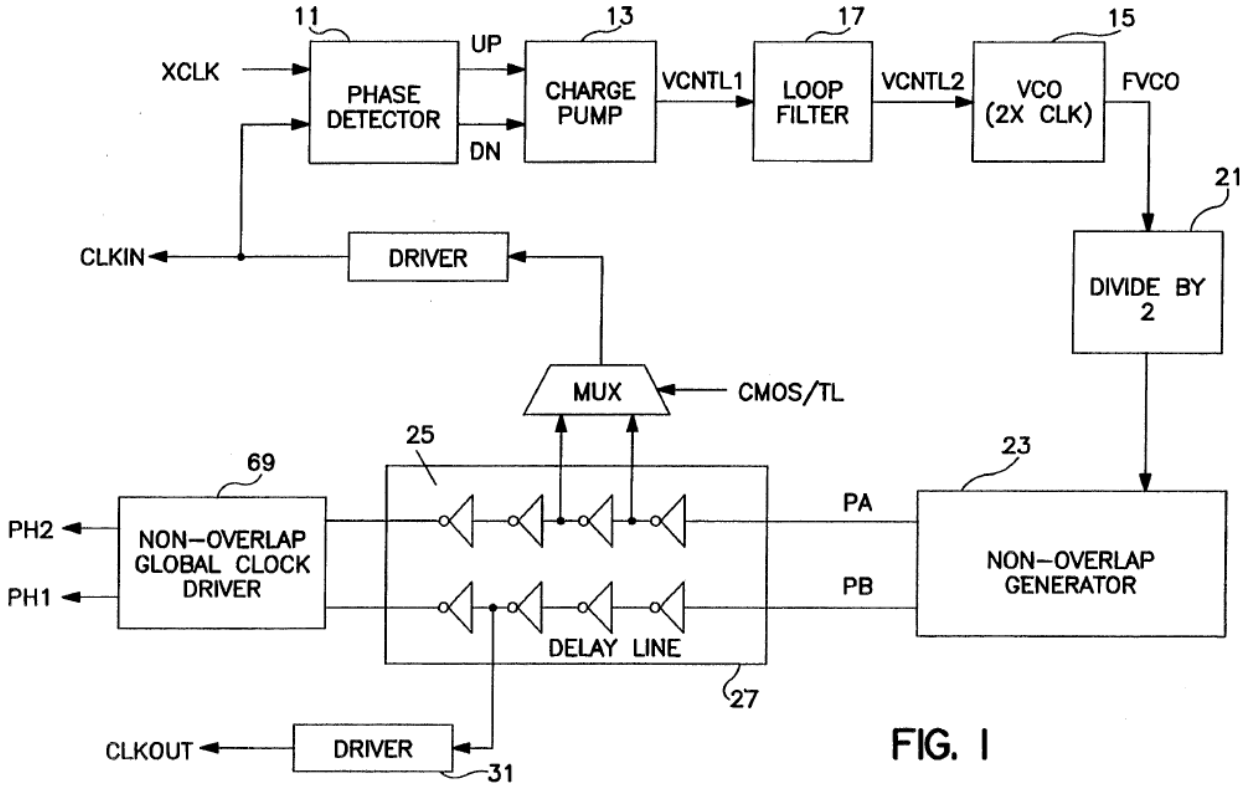


FIG. 1

(Appx528.)

The delay line 27 is a delay circuit that is programmed using a CMOS/TTL control signal. (Appx534 at 4:45-46 ("The delay line can be *programmed* such

that two stages can be added or subtracted from the line.").) Specifically, Young uses a multiplexor ("mux") that accepts the CMOS/TTL control signal to select one of two possible delay values. (Appx528.) The CMOS/TTL control signal is set to either a logic 1 or 0 value (Appx430) and thus comprises binary data that controls the delay of the delay line 27.

The delay line 27 can be programmed via a variety of methods. Young discloses that in one embodiment, a delay value of the delay line 27 is set during manufacturing, such that the delay value cannot be changed subsequently. (Appx534 at 3:67-4:10.) In another embodiment, Young discloses that the delay line 27 is programmed following manufacturing via input pins connected to a system circuit board. (*Id.* at 4:10-14.)

C. The PTAB Proceedings

1. Xilinx's Petition

Xilinx filed its Petition for *inter partes* review of the '122 patent with an accompanying declaration by Donald Alpert, Ph. D. (Appx606-756.)

Xilinx highlighted the extensive admitted prior art described in the '122 patent, which shows, among other things, that "programmable delay circuits" were conventional and not an inventive feature of the patent. (Appx60-63 (discussing the "Conventional PLL" disclosed in Figure 2 of the '122 patent and other portions of the patent describing programmable delay circuits as "conventional").) Xilinx

argued that Nienaber meets all the requirements of the independent claims of the '122 patent but that, "[t]o the extent … the PTAB determines that Nienaber does not expressly disclose a 'programmable delay circuit[,]' … this is disclosed by Young," and thus the '122 patent claims are obvious over a combination of Nienaber and Young. (Appx83; *see generally* Appx82-85.)

Xilinx provided a detailed explanation of why the POSITA would be motivated to combine Nienaber and Young. Both references "disclose delay circuits used within a [phase-locked loop] clock circuit for the same purpose of adjusting the amount of phase shift between a reference clock and a feedback signal." (Appx83.) Moreover, the phase-locked loop clock circuits of the two references are very similar in structure and operation—among other things, "Nienaber discloses *adjustable delay circuits* in the reference and feedback paths," and "Young discloses a *programmable delay element* in the feedback path." (Appx84.) Given these similarities, "it would have been obvious to [the POSITA] to modify the [phase-locked loop] circuit structure of Nienaber … to include the 'programmable' delay element of Young in its reference and feedback paths. Doing so would obtain a predictable result of having 'programmable' delay elements in the reference and feedback paths." (*Id*.)

Dr. Alpert's declaration, as cited in the Petition (Appx84), provided additional reasoning and evidence to support the proposed combination of

Nienaber and Young. (Appx677.) Dr. Alpert did not assert that the precise delay circuit of Young would need to be bodily incorporated into Nienaber. (*See id.*) Rather, Dr. Alpert asserted that the POSITA would be motivated to combine the references because this would enable Nienaber's delay circuits to be programmable in a manner similar to that disclosed in Young (*e.g.*, "by connecting control signals to bonding pads when the microprocessor is packaged or by pins connected to the system's circuit board when the system is operated"). (*Id.*) Dr. Alpert noted that "[t]his could provide an advantage, for example, of allowing the pads to be bonded according to characterization of the design or testing of a manufactured device." (*Id.*)

2. PLL's Preliminary Response

In its Preliminary Response, PLL argued, among other things, that (1) Nienaber does not disclose a "clock" (Appx151-155), (2) the delay taught in Nienaber is not "programmable" (Appx147-150), and (3) the POSITA would not be motivated to combine Nienaber and Young because they are allegedly non-analogous art and would have resulted in an inoperative combination (Appx162-165). Although it quibbled with Xilinx's arguments regarding the disclosure of a "programmable delay circuit" and a "clock" in the prior art, PLL did not propose formal constructions for either term.

3. The Board's Institution Decision

The Board instituted trial to review the patentability of claims 1-10, 12-14, and 16-20 of the '122 patent. (Appx179-214.) The instituted grounds of unpatentability relevant to this appeal are as follows:

> Claims 1-3, 7-10, 14, and 17 as allegedly being unpatentable under 35 U.S.C. § 103 as obvious over Nienaber and Young; and
>
> Claims 4-6, 12, 13, 16, and 18-20 as allegedly being unpatentable under 35 U.S.C. § 103 as obvious over Nienaber, Young, and certain other references.

(Appx212-213.)

While neither Xilinx nor PLL had formally proposed a construction for the term "clock" (*see* Appx66-71; Appx151-155), the Board cited a portion of Dr. Alpert's testimony in construing that term as "a periodic timing control signal." (Appx186-187 (citing Appx651-652).) Applying this construction, the Board found that Nienaber discloses a "clock." (Appx191-192.) The Board further found that Young discloses a "programmable delay circuit" under Xilinx's proposed construction of that term as "a delay circuit that can be programmed, configured, or adjusted to vary its delay time." (Appx196-197 (citing Appx68-69).)

Regarding the proposed combination of Nienaber and Young, the Board rejected PLL's arguments that the references are non-analogous art and would have resulted in an inoperative combination. (Appx194-196.) In finding that the

POSITA would be motivated to combine Nienaber and Young, the Board credited the testimony of Dr. Alpert, stating that "[a]s Dr. Alpert testifies, [modifying Nienaber in view of Young] would allow the desired delay to be configured or programmed by bonding pads or serially loaded from input pads in a manner that is commonly used for a variety of features (*e.g.*, speed selection, functional assignment of I/O pins) during integrated circuit packing assembly or initialization within a functioning system." (Appx195-196 (citing Appx677).)

To further support its finding that the POSITA would be motivated to combine Nienaber and Young, the Board explained that "often it can be routine to use digital components to upgrade existing analog devices." (Appx196 (citing *Western Union Co. v. MoneyGram Payment Sys., Inc.*, 626 F.3d 1361, 1370 (Fed. Cir. 2010); *Leapfrog Enters., Inc. v. Fisher–Price, Inc.*, 485 F.3d 1157, 1161 (Fed. Cir. 2007)).) The Board concluded its motivation-to-combine analysis by noting that "[o]n this record, this articulated reasoning has rational underpinnings and is sufficient to justify the combination of Nienaber and Young." (*Id.*)

4. PLL's Patent Owner Response

In its Patent Owner Response, PLL urged the Board to reject the construction of "clock" provided in the Institution Decision and instead to construe that term as "a periodic signal used for synchronization *in a digital system*."

(Appx249.) To support its argument, PLL cited extrinsic evidence that it had not offered in its preliminary response.[1]

First, PLL argued that the IEEE Dictionary supported its newly proposed narrowing of "clock" to usage in a digital system. (Appx250-254 (citing Appx1182-1194).) After citing multiple definitions of "clock" from that dictionary, PLL concluded that "[f]ocusing on just the definitions directed at a 'clock' signal as a noun … and accepting the broadest definition, that would be '*a periodic signal used for synchronization*.'" (Appx250-251.) PLL recognized that the IEEE Dictionary's definitions of clock do not reference a "digital system" and that the word "digital" does not appear in any of the definitions. (*Id.*) Nonetheless, PLL argued that the words "in a digital system" should be added to the IEEE Dictionary's definition of clock because (1) "all of the definitions of the term 'clock' … are in the 'C' category, which signifies 'computer,'" and (2) the IEEE standards that are the sources of the definitions "are all computer- or digital-based standards." (Appx253.)

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[1] Although PLL notes that it was not permitted to present testimonial evidence without Board authorization when it filed its preliminary response (BlueBr. 16), there were no restrictions on filing other evidence at that time—in fact, PLL filed a dictionary definition for the term "programmable" (Appx1776-1777; Appx1090)—nor did PLL seek Board authorization to file testimonial evidence with its preliminary response. *See* 37 C.F.R. § 42.107(a), (c) (2012).

Second, PLL provided testimony from its expert, Dr. Hayes, in support of its construction of "clock." (Appx251-256 (citing Appx1105-1109).) At deposition, Dr. Hayes stated that there is no such thing as an "analog clock signal," and that clock signals are used only in digital systems. (Appx985.) At the same deposition, however, Dr. Hayes conceded that the "C" category of the IEEE Dictionary may include terms that are "analog or mixed signal." (Appx990-991.)

PLL further argued for the first time that the term "programmable" should be construed as "capable of *storing in memory* data and/or instructions to alter the delay." (Appx260.) Here, too, PLL cited the IEEE Dictionary for the first time in an attempt to support its construction. (Appx262-263.) After referencing multiple definitions of "programmable" from the IEEE Dictionary, PLL concluded that "[t]aking the full breadth of the relevant aspects of" those definitions "leads to the following interpretation of 'programmable' which the Board should adopt: '*capable of accepting data and/or instructions to alter a device's state to perform specific task(s) or to alter its basic function*.'" (Appx263.) Similar to its reliance on the IEEE Dictionary for its construction of clock, PLL acknowledged that the IEEE Dictionary's definitions for programmable do not reference "memory." (*Id.*) Nonetheless, PLL argued that "the definitions refer to the capability of 'accepting' data and/or instructions[,] … and a memory is inherently necessary to accept the data and/or instructions." (Appx263-264.)

PLL argued that Xilinx's obviousness challenges fail because Nienaber does not disclose a "clock" (Appx267-274), and Young does not disclose a "programmable delay circuit" (Appx279-280) under PLL's newly proposed constructions. PLL further argued that the POSITA would not have combined Nienaber and Young because the combination "would have resulted in insufficient granularity for vertically aligning a television or video monitor picture acceptably," and thus the combination would render Nienaber unsatisfactory for its intended purpose. (Appx276-279.)

5. Xilinx's Reply to the Patent Owner Response

In its Reply, Xilinx provided arguments and evidence, including a second declaration from Dr. Alpert, to rebut the arguments made in PLL's Patent Owner Response. (Appx884-913.)

To rebut PLL's contention that all of the "C" category definitions in the IEEE Dictionary are related to strictly digital systems, Xilinx cited other portions of that same dictionary. (Appx317 (citing Appx888-891; Appx953; Appx956; Appx958-959).) The portions cited by Xilinx showed that the "C" category includes definitions for various analog and mixed signal systems and components, including an "analog computer," "hybrid circuit," and "operational amplifier," among others. (*Id*.) In light of the breadth of the category, Xilinx argued that it

would be improper to read the phrase "in a digital system" into the dictionary's definition of "clock," as proposed by PLL. (Appx317-318.)

To rebut Dr. Hayes' contention that there is no such thing as an "analog clock signal" and that clock signals are used only in digital systems, Xilinx cited U.S. Patent Nos. 5,654,657 (Appx1032-1044) and 5,706,004 (Appx1045-1052), both of which expressly disclose "analog clock signals" (Appx319-320).

To rebut PLL's contention that Nienaber does not disclose clock signals because it is a purely analog system (Appx267-274), Xilinx established that Nienaber discloses a hybrid system that uses a digital vertical sync signal for timing control (Appx326-329).

Xilinx established that PLL's proposed constructions of "clock" and "programmable"—both of which were offered for the first time after the Board's Institution Decision—were erroneous (Appx315-324), and that Nienaber and Young meet these claim requirements, as correctly construed (Appx324-334).

Xilinx also rebutted PLL's argument that the combination of Nienaber and Young would render Nienaber unsatisfactory for its intended purpose. (Appx334-338.) Specifically, Xilinx explained that PLL's characterization of Nienaber's intended purpose was unduly narrow (Appx335-337), and that contrary to PLL's argument, the proposed combination of references does not require bodily

incorporation of the precise delay circuit of Young into Nienaber's system (Appx337-338).

6. PLL Responds to Xilinx's Reply in Multiple Ways

After Xilinx filed the Reply and second declaration of Dr. Alpert, PLL elected to take Dr. Alpert's deposition and question him on topics addressed in both the Reply and his declaration. (Appx1371-1425.) PLL subsequently filed a transcript of the deposition with the Board as an exhibit. (*Id.*) PLL also filed eight pages of observations on the cross-examination. (Appx346-355.) At oral argument (Appx379-434), PLL presented arguments on a variety of topics, including the "C" category code of the IEEE Dictionary (Appx413-416) and the patents cited by Xilinx for their disclosure of "analog clock signals" (Appx416-418). At no point did PLL move to strike Xilinx's Reply or to exclude evidence cited in the Reply.

7. The Board's Final Written Decision

In its Final Written Decision, the Board construed the term "clock" as "a periodic signal for timing control (or synchronization)." (Appx12.) The Board concluded that the intrinsic evidence does not support PLL's proposed narrowing of the term to a digital system, nor does the extrinsic evidence "support limiting 'clock' … to use only in digital systems." (Appx8-12.) In particular, the Board found that the IEEE Dictionary's category codes should not "limit the definitions

provided in the IEEE Dictionary…. [because,] as Petitioner demonstrates and Patent Owner's declarant concedes, the 'C' category code is not limited exclusively to 'digital' systems." (Appx11 (citing Appx990-991).) Further, the Board found unpersuasive Dr. Hayes' testimony that clock signals do not have a recognized meaning in analog systems, explaining that "[Xilinx] has offered examples of analog or hybrid analog/digital systems that use a 'clock' signal.' … This [and other extrinsic] evidence suggests that clock signals can be analog as well as digital." (Appx11.)

The Board next construed "programmable delay circuit" as a delay circuit that is "capable of accepting data or instructions, or both, to alter the delay." (Appx17.) The Board concluded that the intrinsic evidence does not support PLL's proposed narrowing of the term to require a "memory," nor does the extrinsic evidence support PLL's proposed construction. (Appx15-17.) Specifically, the Board found that the IEEE Dictionary does not support PLL's proposed construction and that Dr. Hayes' testimony "is conclusory and cites to no evidence that supports his contention. Thus, we give it minimal weight." (Appx16.)

The Board found that the independent claims were obvious over the combination of Nienaber and Young. (Appx23-33.) In so holding, the Board found that Nienaber discloses a "clock" (Appx25-28) and that Young discloses a "programmable delay circuit" (Appx28). The Board also found that the POSITA

would be motivated to combine the references, rejecting PLL's argument that the resulting combination would render Nienaber unsatisfactory for its intended purpose. (Appx28-33.) The Board supported its finding with a detailed explanation, concluding that "when viewed in the context of all of the evidence—the background references, the testimony of the experts, and the admitted prior art, the evidence strongly supports the notion that the circuit Patent Owner claimed was nothing more than the 'combination of familiar elements according to known methods,' 'each performing the same function it had been known to perform,' 'yield[ing] predictable results.'" (Appx33.)

PLL appealed. (Appx435-439.)

SUMMARY OF THE ARGUMENT

The Board's judgment that claims 1-10, 12-14, and 16-20 of the '122 patent are unpatentable should be affirmed for the following reasons.

First, the Board's determination that Nienaber discloses a "clock" is supported by substantial evidence. The Board properly construed the term as "a periodic signal for timing control (or synchronization)." (Appx12.) Neither the intrinsic nor extrinsic evidence support PLL's argument that the term should be limited to a "digital system." The '122 patent does not use the word "digital," and the specification is silent as to whether the phase-locked loop circuit disclosed therein is for use with a digital system or an analog system. (Appx45-50.)

Likewise, the IEEE Dictionary definitions cited by PLL make no mention of a "digital system" and therefore do not support PLL's construction. (*See* Appx250-251 (citing Appx1182-1189).) PLL does not dispute that Nienaber discloses a clock under the Board's correct construction, and the Board's alternate finding that Nienaber discloses a clock even under PLL's proposed construction is supported by substantial evidence.

Second, the Board's determination that Young discloses a "programmable delay circuit" is supported by substantial evidence. The Board properly construed "programmable delay circuit" as a delay circuit "capable of accepting data or instructions, or both, to alter the delay." (Appx17.) PLL's argument that the term requires a memory is not supported by the record. The word "memory" does not appear anywhere in the claims of the '122 patent (Appx50), and the specification even describes embodiments that *do not* use a memory (Appx49 at 4:37-45). Further, the IEEE Dictionary definitions cited by PLL do not refer to a "memory" and therefore do not support PLL's construction. (*See* Appx262-263 (citing Appx1190).) PLL does not dispute that Young discloses a programmable delay circuit under the Board's correct construction.

Third, the Board's determination that a POSITA would have been motivated to combine Nienaber and Young is supported by substantial evidence. The Board correctly determined that adding programmability, as taught by Young, to

Nienaber's adjustable delay circuits would provide advantages that would be recognized by the POSITA. (Appx32-33 (citing Appx677).) The Board also correctly determined that the POSITA would be motivated to update Nienaber's analog components using the more modern digital components disclosed in Young, and that this Court routinely has found such updating to be obvious. (Appx31.) The Board's detailed explanation provides an articulated reasoning with rational underpinning as to why the POSITA would have combined the references. PLL's arguments to the contrary are premised on an erroneous bodily incorporation theory, and the Board correctly rejected them. (Appx30-31.)

Fourth, PLL cannot salvage its claims by arguing that the Board committed procedural errors. PLL had numerous opportunities to respond to Xilinx's Reply, and took advantage of many of them, while choosing to forgo others. PLL's apparent dissatisfaction with the *inter partes* review process is properly directed to Congress and the PTO, not this Court. PLL also argues that the Board supported its obviousness determination with "new rationales" for which PLL was not given notice. The record shows, however, that PLL had notice of all the rationales ultimately relied on by the Board no later than the Board's Institution Decision and had an opportunity to respond to all of them. The Board complied with the APA.

STANDARD OF REVIEW

The ultimate construction of a claim is a legal conclusion that is reviewed de novo, while factual determinations concerning extrinsic evidence underlying claim construction are reviewed for substantial evidence. *In re Cuozzo Speed Techs. LLC*, 793 F.3d 1268, 1279-80 (Fed. Cir. 2015) (citing *Teva Pharms. U.S.A., Inc. v. Sandoz, Inc.*, 135 S. Ct. 831, 841 (2015)).

Whether a patent is obvious is a question of law reviewed de novo, while underlying factual findings are reviewed for substantial evidence. *Crocs, Inc. v. ITC*, 598 F.3d 1294, 1308 (Fed. Cir. 2010). The Board's factual findings—including its findings on the scope and content of the prior art, level of ordinary skill in the art, the differences between the claimed invention and the prior art, and motivation to combine—must be sustained so long as they are based on substantial evidence. *In re Gartside*, 203 F.3d 1305, 1311-13, 1319-20 (Fed. Cir. 2000); *see also Apple Inc. v. Samsung Elecs. Co.*, 839 F.3d 1034, 1051 (Fed. Cir. 2016) (en banc) ("What a prior art reference teaches and whether a skilled artisan would have been motivated to combine references are questions of fact.").

Substantial evidence is "more than a mere scintilla of evidence but something less than the weight of the evidence." *In re Rambus, Inc.*, 753 F.3d 1253, 1256 (Fed. Cir. 2014) (citations and internal quotation marks omitted); *see also Consol. Edison Co. v. NLRB*, 305 U.S. 197, 217 (1938) (substantial evidence

"means such relevant evidence as a reasonable mind might accept as adequate to support a conclusion"). "[W]here two different, inconsistent conclusions may reasonably be drawn from the evidence in record, an agency's decision to favor one conclusion over the other is the epitome of a decision that must be sustained upon review for substantial evidence." *In re Jolley*, 308 F.3d 1317, 1329 (Fed. Cir. 2002).

The Court reviews the Board's procedures for compliance with the Administrative Procedures Act. *Belden, Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1080 (Fed. Cir. 2015). "Under that statute, [the Court] set[s] aside actions of the Board that are arbitrary, capricious, an abuse of discretion, or otherwise not in accordance with law." *Veritas Techs. LLC v. Veeam Software Corp.*, 835 F.3d 1406, 1413 (Fed. Cir. 2016) (quoting 5 U.S.C. § 706(2)(A)). The Board's evidentiary rulings also are reviewed for abuse of discretion, *see Belden*, 805 F.3d at 1078, whereas the narrow question of whether "a ground the Board relied on was 'new,' requiring a new opportunity to respond, is a question of law, subject to de novo review." *In re NuVasive, Inc.*, --- F.3d ----, 2016 WL 6608999, at *4 (Fed. Cir. Nov. 9, 2016).

ARGUMENT

I. THE BOARD CORRECTLY FOUND THAT THE CLAIMS OF THE '122 PATENT ARE OBVIOUS

In finding claims 1-10, 12-14, and 16-20 of the '122 patent obvious over the combination of Nienaber and Young (and other references for some claims), the Board correctly construed the terms "clock" and "programmable delay circuit," and the Board's findings that the prior art meets these requirements are supported by substantial evidence. Substantial evidence also supports the Board's finding that the POSITA would have been motivated to combine Nienaber and Young. Accordingly, the Board's judgment should be affirmed.

A. The Board's Determination that Nienaber Discloses a Clock Is Supported by Substantial Evidence.

The Board found that Nienaber discloses a "clock," as recited in the claims of the '122 patent. (Appx25-28.) The Board correctly construed this term, and PLL does not dispute that substantial evidence supports the Board's finding that Nienaber discloses a clock under the Board's construction. Moreover, the Board's alternate finding that Nienaber discloses a clock under PLL's proposed construction also is supported by substantial evidence.

1. The Board Correctly Construed the Term "Clock."

In the Final Written Decision, the Board correctly construed "clock" as "a periodic signal for timing control (or synchronization)." (Appx12.) PLL does not dispute this basic construction, but instead argues that clocks are not used in analog

systems, and thus the term "clock" should be construed as "a periodic signal used for synchronization *in a digital system*." (Appx249; BlueBr. 39-45.) Contrary to PLL's argument, neither the claims nor the specification of the '122 patent require a "digital system," and thus the intrinsic evidence does not support PLL's narrow construction. Moreover, substantial evidence supports the Board's factual findings regarding the IEEE Dictionary and other extrinsic evidence. PLL's challenge to the Board's claim construction lacks merit.

a) A "Digital System" Is Not Required by the Intrinsic Evidence.

PLL argues that the Board's construction of "clock" is unreasonably broad and that the term should be limited to use "in a digital system." (Appx249-259; BlueBr. 39-45.) But the claims of the '122 patent do not recite a "digital system." (Appx50.) In fact, at oral argument, PLL conceded that each of the elements of independent claim 1 (*i.e.*, "oscillator," "reference path," "feedback path," and "delay circuit[s]") is found in both analog and digital phase-locked loops. (Appx420-421.) Nothing in the claims requires a "digital system."

Nor is PLL's proposed narrowing of the term "clock" to require a "digital system" supported by the specification. Throughout the '122 patent, clocks are described broadly as periodic signals used for timing control. (Appx48 at 1:19-35 (describing a clock synthesizer as generating an output clock based on an input clock, where both input and output clocks are periodic signals having "cycles"); *id.*

at 2:45-3:20 (discussing clock signals as periodic signals).) No portion of the '122 patent indicates that clocks can only be used in digital systems. As with the claims, the word "digital" does not appear anywhere in the specification of the '122 patent. (Appx45-50; Appx983.)

PLL argues that the '122 patent describes only a digital embodiment, and that the claims should therefore be limited to the context of a digital system. (BlueBr. 39.) But the patent is not limited to a digital context. The '122 patent describes a circuit based on a phase-locked loop (*see*, *e.g.*, Appx48 at 1:10-15; Appx49 at 3:30-39) and does not indicate whether the phase-locked-loop circuit is for use with a digital system or an analog system.

Further, assuming *arguendo* that the specification only teaches a digital embodiment, that still is not enough to limit the claims to the single embodiment disclosed in the specification. PLL has not demonstrated a clear intention to limit the clock to use in a digital system, and thus PLL's construction impermissibly imports limitations into the claims. *See Superguide Corp. v. DirecTV Enter., Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004) ("Though understanding the claim language may be aided by the explanations contained in the written description, it is important not to import into a claim limitations that are not a part of the claim.").

This Court "has expressly rejected the contention that if a patent describes only a single embodiment, the claims of the patent must be construed as being

limited to that embodiment." *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004). "Even when the specification describes only a single embodiment, the claims of the patent will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope 'using words or expressions of manifest exclusion or restriction.'" *Id.* (quoting *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1327 (Fed. Cir. 2002)). Such words or expressions of manifest exclusion or restriction may be found, for example, in explicit disclaimers and express limiting definitions included in the specification and in statements made during prosecution. *See Liebel-Flarsheim*, 358 F.3d at 906-08 (citing cases).

In cases where claim language is limited based on a single embodiment disclosed in the specification, this Court has made clear that the claim language is limited not because the specification failed to describe a broader embodiment, but rather because the specification, claim, or prosecution history made clear that the invention was limited in a certain manner. *Liebel-Flarsheim*, 358 F.3d at 907-08; *see also Toro Co. v. White Consol. Indus., Inc.*, 199 F.3d 1295, 1301 (Fed. Cir. 1999) (claims limited when specification described structure as being "important to the invention"); *Modine Mfg. Co. v. U.S. Int'l Trade Comm'n*, 75 F.3d 1545, 1551 (Fed. Cir. 1996) (claims limited to particular numerical range when broader range was surrendered during prosecution by amendment of the specification).

Here, neither the specification nor the prosecution history of the '122 patent describes the clock as being limited to the alleged digital embodiment described in the specification. PLL has not demonstrated a clear intention, using words or expressions of manifest exclusion or restriction, to limit the claim scope in this manner. Thus, PLL's proposed narrowing of the term "clock" based on the alleged digital embodiment of the specification improperly reads limitations into the claims.

PLL's reliance on *In re Man Machine Interface Technologies LLC*, 822 F.3d 1282 (Fed. Cir. 2016), is misplaced. In that case, the Court considered the Board's construction of the claim language "thumb switch being adapted for activation by the human thumb" to include switch activation by another digit or item so long as the switch is capable of being enabled by a user's thumb. *Id.* at 1285. In rejecting the Board's construction as "unreasonable" and "overly broad," the Court first considered the claim language, noting that it "expressly requires a *thumb* switch, not a *finger* switch," and that the "claim goes on to further require that the thumb switch be 'adapted for activation by a human thumb.'" *Id*. at 1286-87. The Court then highlighted the specification's repeated statements of restriction, finding that such statements presented a "clear teaching" that the patentee intended to limit the "thumb switch" to being made or designed for activation by a human thumb. *Id.*

The intrinsic evidence here lacks both features that led the Court to narrow the claim language in *Man Machine Interface*. First, the '122 patent claims lack express, limiting claim language. In fact, the claims here include no indication—express or otherwise—that the claims should be limited to a "digital system." (*See* Appx50; Appx420-421 (PLL acknowledging at oral argument that the features of independent claim 1 are found in both analog and digital phase-locked loops).) Second, the specification of the '122 patent lacks a "clear teaching" of restriction to a digital system. The word "digital" appears nowhere in the '122 patent specification, which is silent regarding whether its disclosed circuit is for use with a digital or analog system.

PLL's argument based on the prosecution history also fails. PLL alleges that during prosecution of the '122 patent, the Examiner only cited art relating to digital computers, and that this supports its proposed construction. (BlueBr. 41-42.) But Examiners cannot limit claim scope—only an applicant can do that. *See*, *e.g.*, *Sorensen v. Int'l Trade Comm'n*, 427 F.3d 1375, 1378-79 (Fed. Cir. 2005); *Salazar v. Procter & Gamble Co.*, 414 F.3d 1342, 1345 (Fed. Cir. 2005); *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1124 (Fed. Cir. 2004) ("[I]t is the applicant, not the examiner, who must give up or disclaim subject matter that would otherwise fall within the scope of the claims."). And the

Examiner does not have the same incentive as an adversary in litigation to uncover prior art beyond the scope of that offered by an applicant.

In short, PLL's proposed narrowing of the term "clock" is not supported by the '122 patent or its prosecution history. The Board correctly analyzed the intrinsic evidence in rejecting PLL's proposed construction.

b) The Board's Factual Determinations Regarding the Extrinsic Evidence are Supported by Substantial Evidence.

The Board's rejection of PLL's proposed construction of "clock" based on the intrinsic evidence is buttressed by extrinsic evidence. The Board considered extrinsic evidence presented by both parties, finding that the evidence did not support PLL's narrow construction. (Appx10-12.) Substantial evidence supports the Board's findings. *In re Cuozzo*, 793 F.3d at 1279-80.

First, PLL argues that the IEEE Dictionary supports its proposed narrowing of clocks to use in digital systems. (Appx250-254; BlueBr. 42-44.) But the IEEE Dictionary, *PLL's own evidence*, fails to support that proposed construction. The IEEE Dictionary's definitions for clock (Appx250-251 (citing Appx1182-1189)) do not refer to a "digital system," and the word "digital" does not appear in any of the definitions. In fact, based on the several IEEE Dictionary definitions of "clock" cited in its Patent Owner's Response, PLL concluded that "the broadest definition … would be 'a periodic signal used for synchronization.'" (Appx251.) Absent

from this "broadest definition" is the word "digital" or the requirement of a "digital system."

PLL nonetheless argues that because "all of the [IEEE Dictionary's] definitions of the term 'clock' … are in the 'C' category, which signifies 'computer,'" all definitions in that category are related to digital systems, and thus the words "in a digital system" should be added to the definition of clock. (Appx251-254.) But the "C" category includes definitions for various analog and mixed signal systems and components, including "analog computer," "hybrid circuit," and "operational amplifier," among others. (Appx317 (citing Appx888-891; Appx953; Appx956; Appx958-959).) PLL's argument thus fails to recognize the breadth of the "C" category—not all of its definitions are related to digital systems. In light of this breadth, it would be improper to read the phrase "in a digital system" into the dictionary's definitions of "clock."

In reaching its conclusion that the extrinsic evidence presented by PLL and Xilinx "does not support limiting 'clock' … to use only in digital systems" (Appx10-12), the Board properly considered the IEEE Dictionary and its category codes. It "agree[d] with [PLL] that the category codes and corresponding standards can provide useful context," but was not persuaded that the 'category codes' and the standards to which they correspond necessarily limit the definitions in the IEEE Dictionary." (Appx11.) Rather, "as [Xilinx] demonstrates and

[PLL's] declarant concedes, the 'C' category code is not limited exclusively to 'digital' systems. (*Id.*) Thus, far from "wrongly discredit[ing] the category codes and source documents for the term 'clock' in the IEEE Standard Dictionary" (BlueBr. 42), the Board considered the extrinsic evidence regarding the category codes and found that the evidence did not support PLL's narrow construction. That finding is supported by substantial evidence.

PLL also argues that "[t]he Board nonetheless improperly discounted [PLL's IEEE Dictionary] evidence because another IEEE dictionary document, the IEEE Computer Glossary, has a broader coverage and includes some terms that relate to 'Analog computer concepts' and 'General terms—electrical.'" (BlueBr. 42.) According to PLL, this "conclusion was improper because the IEEE Standard Dictionary and the IEEE Computer Glossary are different documents." (*Id.*) In fact, the Board's Final Written Decision never even mentions the IEEE Computer Glossary, whereas it discusses the IEEE Dictionary extensively.

That is entirely consistent with the evidence presented by the parties. To rebut PLL's citations to the IEEE Dictionary in its Patent Owner's Response (Appx250-254), Xilinx cited other parts of the same IEEE Dictionary (Appx317 (citing Appx953; Appx956; Appx958-959)). Xilinx did not cite or refer to the IEEE Computer Glossary in its Reply, and the only discussion of the IEEE Computer Glossary in the IPR proceeding is found in a single paragraph of Dr.

Alpert's second declaration. (Appx891.) At oral argument, the Board questioned the parties on the IEEE Dictionary extensively (*see*, *e.g.*, Appx387-391; Appx411-417), while the IEEE Computer Glossary was not discussed. Nothing in the record supports PLL's argument that the Board "improperly discounted" the IEEE Dictionary evidence in favor of the IEEE Computer Glossary evidence.

In any event, the IEEE Computer Glossary was properly offered in rebuttal to the Patent Owner Response and constitutes additional evidence in support of the Board's finding. As Dr. Alpert testified, many definitions in the "C" category of the IEEE Dictionary are from the IEEE Computer Glossary. (Appx891.) The definitions of the IEEE Computer Glossary relate to "computers," as the title indicates, but the definitions are not limited to digital systems. (*Id.*) Rather, as the IEEE Computer Glossary describes its own scope, "[t]his glossary defines terms pertaining to computer hardware. It includes terms from … areas," including "general circuit concepts" and "analog computer concepts." (Appx781.) The broad scope of the IEEE Computer Glossary, which is the source of many of the definitions from the "C" category of the dictionary, is further evidence supporting the Board's finding that the IEEE Dictionary evidence does not support PLL's proposed construction.

Second, the Board's factual findings regarding Dr. Hayes' testimony and Xilinx's rebuttal evidence (Appx11) also are supported by substantial evidence.

Dr. Hayes stated that there is no such thing as an "analog clock signal," and that clock signals are not used in analog systems. (Appx985.) Dr. Hayes is incorrect. For example, U.S. Patent Nos. 5,654,657 (Appx1032-1044) and 5,706,004 (Appx1045-1052), cited by Xilinx during the proceeding, both disclose analog clock signals. (Appx319-320; Appx892-894 (Dr. Alpert discussing the disclosures of these patents).)

PLL argues that these patents were "cherry-picked" by Xilinx (BlueBr. 43) and that they are "aberrations" (Appx416-417) not representative of usage in the art. Xilinx disagrees, as it stated at oral argument. (Appx432 (explaining that "there are many other references like that").) In any event, PLL's only evidence that these patents are "aberrations" is the conclusory testimony of its expert, Dr. Hayes. (BlueBr. 44 (citing Appx1108-1109).) For example, Dr. Hayes states that "[t]he term 'clock' does not have an established and standardized meaning in analog circuits" (Appx1108), but he cites no authority to support this assertion. Such "conclusory, unsupported assertions by experts as to the definition of a claim term are not useful to a court." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1318 (Fed. Cir. 2005).

In the Final Written Decision, the Board considered Dr. Hayes' testimony and PLL's rebuttal evidence, finding Dr. Hayes' testimony "unpersuasive. [Xilinx] has offered examples of analog or hybrid analog/digital systems that use a 'clock'

signal…. [Xilinx's extrinsic evidence] … counsels against [PLL's] interpretation of the extrinsic evidence." (Appx11.) That finding, like the Board's findings regarding the IEEE Dictionary, is supported by substantial evidence.

2. PLL Does Not Dispute that Nienaber Discloses a Clock Under the Board's Construction.

PLL does not dispute that Nienaber discloses a "clock" as construed by the Board, instead arguing only that Nienaber fails to disclose a clock under its erroneous construction that narrows a clock to use in a "digital system." (BlueBr. 56-59.) Thus, the Court must affirm the Board's finding that Nienaber discloses a clock upon affirming the Board's claim construction. Substantial evidence supports that finding in any event. (*See, e.g.*, Appx272-273 (PLL conceding that Nienaber's "incoming vertical sync signal is a periodic signal for synchronization or timing control"); Appx1115 (PLL's expert acknowledging that Nienaber's incoming vertical sync signal meets the Board's definition of clock signal); Appx72-78 (Xilinx's Petition); Appx324-325 (Xilinx's Reply).)

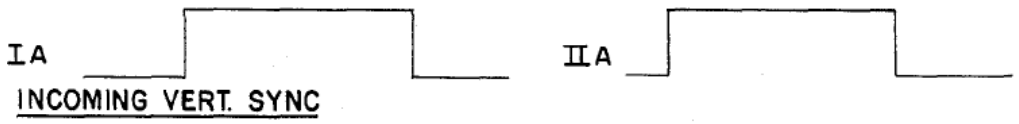
3. Even Under PLL's Erroneous Construction, Nienaber Discloses a Clock.

In its Final Written Decision, the Board found that "even if the 'clock' was required to be digital, we are persuaded that Nienaber would still teach or suggest this limitation." (Appx26.) This finding also is supported by substantial evidence,

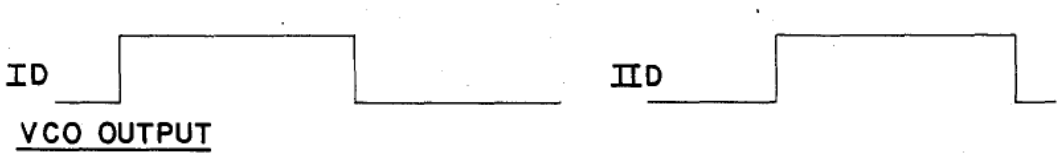
and is an alternate basis to affirm the Board's determination that Nienaber discloses a clock.

Nienaber states that the circuitry shown in Figure 1 may be used in a computer monitor or television. (Appx525 at 3:34-42.) That circuitry receives, processes, and generates digital signals, and thus uses digital modes of operation, techniques, or components. (Appx900-906 (Alpert Declaration).) Nienaber's Figures 1 and 2 illustrate this. (Appx523.)

Figure 1 shows that an incoming vertical sync signal is received on a line 10 and processed by Nienaber's system. (*Id.*) Waveforms IA and IIA of Figure 2, which illustrates signals from various points in the circuitry of Figure 1, show that the incoming vertical sync signal is digital because the signal takes on discrete values, rather than reflecting the continuous slopes of an analog signal:



(*Id.*; *see also* Appx900-902.) Nienaber's system processes the digital incoming vertical sync signal and generates an output on line 22 that is a digital signal. This is shown in waveforms ID and IID of Nienaber's Figure 2, which represent "the VCO output on line 22" (Appx525 at 4:39, 4:67):



(Appx523; *see also* Appx900-902.)

Substantial evidence supports the Board's finding that Nienaber discloses a clock "even if the 'clock' was required to be digital." (Appx26.) Dr. Hayes conceded at his deposition that the waveforms of the vertical sync signal shown in Figure 2 of Nienaber are digital (Appx1001), and that vertical sync signals used in televisions and computer monitors at the time of Nienaber's invention were digital (Appx1002-1003). Further, the Board credited the "persuasive[]" testimony of Dr. Alpert that "some televisions … near the date of invention of Nienaber[] were hybrid systems including both digital and analog components and techniques. Dr. Alpert supports his testimony with extensive citation to and explanation of Nienaber and various prior art references from that time, and thus, we find that his testimony is entitled to substantial weight." (Appx26.) The testimony of Dr. Hayes and Dr. Alpert and the numerous references cited by Dr. Alpert provide substantial evidence to support the Board's finding.

PLL argues that even if Nienaber's vertical sync signal is a digital signal, "Xilinx failed to prove that his vertical sync signal is a 'clock' for any digital components. *Only if the vertical sync signal were used to … pulse synchronous digital circuits* … could that vertical sync signal be considered a 'clock.'" (BlueBr.

57.) But that is not the construction PLL proposed. PLL's proposed construction broadly requires that the clock signal be "used for synchronization in a digital system." (Appx249.) That construction does not require that the clock signal be used more narrowly to "pulse synchronous digital circuits." PLL waived this substantially narrower claim construction. *See Digital-Vending Servs. Int'l, LLC v. Univ. of Phoenix, Inc.*, 672 F.3d 1270, 1273-74 (Fed. Cir. 2012). Thus, the Board's finding is supported by substantial evidence even if Nienaber's vertical sync signal is not used to pulse synchronous digital circuits.

B. The Board's Determination that Young Discloses a Programmable Delay Circuit Is Supported by Substantial Evidence.

The Board found that Young discloses a "programmable delay circuit," as recited in the claims of the '122 patent. (Appx28.) As described below, the Board correctly construed this claim term, and PLL does not dispute that substantial evidence supports the Board's determination that Young discloses a programmable delay circuit under the Board's construction.

1. The Board Correctly Construed the Term "Programmable Delay Circuit."

In the Final Written Decision, the Board correctly construed "programmable delay circuit" as a delay circuit "capable of accepting data or instructions, or both, to alter the delay." (Appx17.) PLL argues that the term "programmable" should be construed as "capable of *storing in memory* data and/or instructions to alter the

delay." (Appx260.) But neither the claims nor the specification of the '122 patent require a "memory," and thus the intrinsic evidence does not support PLL's construction. Further, substantial evidence supports the Board's factual findings regarding the IEEE Dictionary and other extrinsic evidence. *In re Cuozzo*, 793 F.3d at 1279-80. The Court should affirm the Board's construction.

a) The Intrinsic Evidence Does Not Require a "Memory" for Programming a Programmable Delay Circuit.

PLL argues that the claims require a "memory" that is "capable of storing … data and/or instructions" for programming a programmable delay circuit. (Appx260.) But the claims of the '122 patent do not require a "memory" and, in fact, the word "memory" is absent from the claims. (Appx50.)

Nor does the specification of the '122 patent require a memory for programming a programmable delay circuit. (*See* Appx895-896.) As correctly noted by the Board, all discussions in the '122 patent specification regarding the use of memory "make clear that the memory is an optional component and is not required." (Appx16.) Specifically, the specification uses permissive, rather than restrictive, language in describing the memory. (*See, e.g.*, Appx48 at 2:24-33 ("*may be* stored in a … memory"); *id.* at 2:45-48 ("*can be* made user-programmable, through programmable memory, Serial interface, *or* hardware inputs"); Appx49-50 at 4:55-5:4 ("*may be* stored in" memory).) This permissive language indicates the disclosure is not meant to be limited to programming that

requires information stored in memory. *See Prolitec, Inc. v. Scentair Techs., Inc.*, 807 F.3d 1353, 1358 (Fed. Cir. 2015) ("[T]he use of 'may' signifies that the inventors did not intend to limit [the claim] ….").

PLL's focus on statements within the '122 patent specification "specify[ing] that 'the present invention' has memory of one form or another" (BlueBr. 62) ignores that the specification also describes embodiments of the "present invention" that *do not* use a memory. Specifically, the '122 patent states that the "present invention" is shown in Figure 2. (Appx49 at 3:21-24.) In describing Figure 2, the '122 patent states that the "control logic" (also referred to as the "logic block") may include memory for controlling programmable delay circuits. (Appx49-50 at 4:55-5:4.) The '122 patent further describes, however, that the programmable delay circuits may be controlled *without* the use of a memory. (*See* Appx49 at 4:37-45.) Specifically, the specification describes that delay times of a programmable delay circuit can be "one-time programmable" when set by various means, including blowing "fuses" and changing "metal-masks," which do not expressly require a memory. (Appx49 at 4:37-45.)

In fact, there is no intrinsic evidence establishing that a memory is required to program delay times by using fuses and metal-masks. And, as discussed below, substantial evidence supports the Board's finding based on the extrinsic evidence "that programming may be done without a memory," including by "using fuses or

metal masks." (Appx17 (citing Appx895-896 ¶¶ 17-19; Appx619 ¶ 33; Appx624-626 ¶ 43).)

b) The Board's Factual Findings Based on Extrinsic Evidence are Supported by Substantial Evidence.

PLL relies on two types of extrinsic evidence to contradict the Board's finding that a "programmable delay circuit" does not require memory—Dr. Hayes' testimony and the IEEE Dictionary. Neither supports PLL's position.

First, in disputing the Board's finding that programming may be accomplished without memory, PLL argues that "[e]ven when fuses or metal masks are utilized, the configuration bits would still be stored in a memory…." (BlueBr. 61.) But PLL's attorney argument is contradicted by the evidence. Xilinx's expert testified that when fuses and metal masks are used to program a programmable delay circuit in the '122 patent, a memory is neither used nor required. (Appx619; Appx624-626; Appx895; Appx1289-1290 (Dr. Alpert's declarations and deposition testimony describing programming of delay circuit without memory using fuses and metal masks).) This evidence is consistent with testimony from PLL's expert, Dr. Hayes, who explained that a programmable delay circuit could be programmed by using "an array of fuses that control the inputs being applied to the circuit and by selectively blowing or not blowing the fuses, creat[ing] a different input pattern, which could be applied to the circuit in

question." (Appx997.) Dr. Hayes' testimony confirms that when fuses are used to program a programmable delay circuit, a memory is not necessary.

Although PLL argues that "fuses … do not imply the absence of memory," its citations to Dr. Hayes' deposition transcript do not establish that a memory is required when fuses are used. (BlueBr. 61 (citing Appx996-998).) Regardless of whether "fuse-based memory devices" exist (Appx997), Dr. Hayes never testified that a memory is necessary to program a delay using fuses.[2] PLL cites no other evidence to support its attorney argument, which cannot overcome the evidence of record.

Second, notwithstanding PLL's argument that the IEEE Dictionary supports its proposed narrowing of "programmable delay circuits" to require a memory (Appx262-263), the IEEE Dictionary's definitions for "programmable" (*id.* (citing Appx1190)) do not refer to a "memory." In fact, in its Patent Owner Response, PLL relied on several definitions of "programmable" from the dictionary to support a proposed definition of "capable of accepting data and/or instructions to

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[2] Dr. Hayes' testimony regarding fuses contrasts starkly with his conclusory, unsupported assertion that a metal mask is used in conjunction with a memory to program a programmable delay circuit. (Appx997-998.) The Board was entitled to credit Dr. Alpert's testimony over Dr. Hayes' testimony regarding both fuses and metal masks, but the fact remains that Dr. Hayes did not testify, even in a conclusory fashion, that a memory is *required* when fuses are used.

alter a device's state to perform specific task(s) or to alter its basic function." (Appx262-263.) A "memory" is absent from that proposed definition.

PLL argues that while the IEEE Dictionary definitions do not explicitly refer to memory (Appx263-265), "memory is necessary to accept data or instructions and thus be 'programmable.'" (BlueBr. 60.) The only evidence provided by PLL to support its argument is Dr. Hayes' conclusory, unsupported assertion that "[t]he IEEE definition refers to the capability of 'accepting' data and/or instructions (IEEE Dictionary at 826), and a memory is inherently necessary to accept the data and/or instructions. The 'data and/or instructions' is the programming by which the device is 'programmable.'" (Appx1110.) The Board correctly concluded that this testimony "is conclusory and cites to no evidence that supports his contention. Thus, we give it minimal weight." (Appx16.)

Moreover, PLL's argument that memory is necessary to accept data or instructions is incorrect. (*See* Appx896-897.) As explained above, the '122 patent describes that a delay time of a programmable delay circuit can be set by various means that do not require a memory, including blowing fuses and changing a metal mask. (Appx49 at 4:37-45.) Under such techniques, data or instructions for setting the delay time are accepted by the fuses or metal mask, and a memory is not required. (*Id.*; Appx619; Appx624-626; Appx895; Appx1289-1290.)

The Board properly considered the IEEE Dictionary and testimonial evidence offered by PLL and found that it did not support PLL's improperly narrow construction for "programmable delay circuit." (Appx15-16.) Substantial evidence supports the Board's findings regarding this extrinsic evidence, and thus the findings should be affirmed.

2. PLL Does Not Dispute that Young Discloses a Programmable Delay Circuit Under the Board's Construction.

PLL does not dispute that Young discloses a "programmable delay circuit," as construed by the Board, instead arguing only that Young fails to disclose that element under its erroneous construction by which a "memory" is required. (BlueBr. 64.) Thus, the Court must affirm the Board's finding that Young discloses a programmable delay circuit (Appx28) upon affirming the Board's claim construction. In any event, substantial evidence supports that finding. (*See* Appx534 at 4:45-46 (Young's disclosure of delay line 27 as "programmed"); Appx430 (PLL's concession that Young's delay line 27 is programmed using a CMOS/TTL control signal that is set to either a logic 1 or 0 value); Appx82-85 (Xilinx's Petition); Appx324; Appx330-334 (Xilinx's Reply).)

C. The Board's Determination that the POSITA Would Have Been Motivated to Combine Nienaber and Young Is Supported by Substantial Evidence.

The Board correctly found that the POSITA would have been motivated to combine Nienaber and Young. Specifically, the Board found that modifying Nienaber in view of Young would allow a desired delay to be configured or programmed in a manner commonly used for a variety of features during integrated circuit packing assembly or initialization within a functioning system. (Appx32-33 (citing Appx677).) The Board further recognized that the POSITA would have been motivated to "update[] those analog components [of Nienaber] using more modern digital components, as taught in Young," emphasizing that this Court "routinely has found such updating to be obvious." (Appx31-32 (citing *Muniauction, Inc. v. Thomson Corp.*, 532 F.3d 1318, 1326-27 (Fed. Cir. 2008); *Leapfrog*, 485 F.3d at 1161-62; *DyStar Textilfarben GmbH & Co. Deutschland KG v. C. H. Patrick Co.*, 464 F.3d 1356, 1368 (Fed. Cir. 2006)).) These findings are supported by the substantial evidence cited in the Final Written Decision. PLL's arguments do not compel a different conclusion.

1. The Combination of Nienaber and Young Would Not Render Nienaber Insufficient for Its Intended Purpose.

PLL argues that the POSITA would not have combined Nienaber and Young because the combination would render Nienaber unsatisfactory for its intended purpose. (BlueBr. 65-69.) According to PLL, the combination of Nienaber and

Young would "yield[] a grand total of only four possible delays – too few to achieve Nienaber's primary purpose, which is vertically centering a television picture." (*Id.* at 65-66.)

As correctly recognized by the Board in its Final Written Decision, PLL's identification of Nienaber's intended use is too narrow. (Appx29.) Although Nienaber states that its system may be used for vertically aligning a television or video monitor picture, the reference more broadly discloses the use of a phase-locked loop and adjustable delay circuits for shifting a video display in both up and down directions without undesirable side effects. (Appx524 at 2:23-24; *see also id.* at 2:3-14 (describing undesirable side effects of conventional methods).)

That the intended purpose of Nienaber is broader than "vertically aligning a television or video monitor picture acceptably" is evident throughout Nienaber's disclosure.

- Nienaber states that a "principal object" of its system is to permit adjustably shifting video information in either vertical direction. (Appx525 at 3:57-62.)
- Nienaber's "Detailed Description" begins by identifying the broad intended purpose of the disclosure—advancing or delaying vertical retrace without creating undesirable side effects. (Appx524 at 2:55-58.)
- Without reference to vertical video centering applications, Nienaber's Abstract states broadly that a "phase shifting means" is provided. (Appx522.) The phase shifting means is used for the purpose of "altering the phase relationship between a vertical sync signal … and video information in a video display environment." (*Id.*)

- The Abstract further states that in the disclosed system, an output signal lags or leads an input vertical sync signal based on first and second delay values, and that a video display picture (i) is shifted downward when the output signal leads the input signal, and (ii) is shifted upward when the output signal lags the input signal. (*Id.*)

Substituting the "adjustable" delay circuits disclosed in Nienaber with the "programmable" delay circuits disclosed in Young would not render Nienaber unsatisfactory for its intended purpose of enabling video information to be shifted both up and down on a video display without undesirable side effects. (Appx29.) Rather, by adjusting one or both of the delay values of Young's programmable delay circuits within the system of Nienaber, a video display could be shifted both up and down without undesirable side effects. (*See* Appx336-337.)

PLL argues that one of the "undesirable side effects" that Nienaber attempts to overcome is a misaligned picture, and therefore the combination of references renders Nienaber unsatisfactory for its intended purpose. (BlueBr. 66.) But Nienaber expressly identifies the "undesirable side effects" that its invention attempts to overcome, and a misaligned picture is not one of them. (Appx524 at 1:61-63 ("undesirable effects on the linearity of the system and may be unsafe when accessible to the consumer"); *id.* at 2:24-25 ("undesirable side effects on product safety, picture linearity, video bandwidth or video definition").) Further, Nienaber states that the conventional methods already are able to provide vertical video centering. (*See*, *e.g.*, *id.* at 1:55-57; *id.* at 1:64-65; *id.* at 2:15-16.)

Accordingly, PLL's argument that a misaligned picture is an undesirable side effect to be overcome by Nienaber's invention lacks merit.

2. PLL's Argument Is Based on an Erroneous "Bodily Incorporation" Theory.

In the IPR proceeding, the Board correctly determined that PLL's "argument appears to be premised … on an erroneous assumption that the delay elements of Young would be bodily incorporated into the circuit of Nienaber." (Appx30.) But, as recognized by the Board, "'the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into'" another reference to produce the claimed subject matter. *Allied Erecting & Dismantling Co., Inc. v. Genesis Attachments, LLC*, 825 F.3d 1373, 1381 (Fed. Cir. 2016) (quoting *In re Keller*, 642 F.2d 413, 425 (C.C.P.A. 1981)). Rather, "the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art." *Keller*, 642 F.3d at 425; *see also MCM Portfolio LLC v. Hewlett-Packard Co.*, 812 F.3d 1284, 1294 (Fed. Cir. 2015). The Board correctly found that "Young's teaching of 'programmable' delay circuits is sufficient to suggest to a person of ordinary skill that 'programmable' delay circuits could be substituted [into Nienaber], not just the precise circuit disclosed in Young." (Appx30.)

The Board noted that its findings rested "on fundamental obviousness principles. In an obviousness analysis, we do not ignore the modifications that one [of] skill in the art would make to a device borrowed from the prior art." (*Id*.)

"The evidence submitted by [PLL] to support its construction of 'programmable' and the admitted prior art in the '122 patent demonstrates not only that Young's teachings would suggest more to a person of ordinary skill than Patent Owner contends, but also that it was well within the level of skill of a person of ordinary skill in this art to make any modifications necessary." (Appx31.) In other words, even if a bodily incorporation of the precise circuit disclosed by Young into Nienaber would not produce optimal results, the POSITA would nonetheless be motivated to combine the references, and it would be within the level of skill of the POSITA to modify the circuit of Young as necessary to achieve a satisfactory result. This is a textbook Section 103 analysis, applying black-letter law.

To further support its finding, the Board noted that the '122 patent labels "programmable delay circuits" as conventional. (Appx31.) Thus, the '122 patent "serve[s] to document the knowledge that skilled artisans would bring to bear in reading" Young. (*Id.*) Put another way, the POSITA's familiarity with programmable delay circuits further evidences that it would be within the level of skill of the POSITA to modify Young as necessary to achieve a satisfactory result.

Relying solely on an excerpted portion of a sentence in Dr. Alpert's declaration—"'the programmable delay line (27) of Young could be simply substituted for delay circuits (12, 16) of Nienaber'"—PLL argues that "bodily incorporation … is exactly what Xilinx proposed." (BlueBr. 67 (quoting

Appx674-675).) But this excerpt does not, in isolation or in its proper context, propose bodily incorporation.

To begin, the excerpted portion—viewed in isolation—does not state or imply that Young's delay line 27 must be substituted into Nienaber *without modification*. Moreover, the immediately surrounding context of the excerpted portion confirms that Dr. Alpert's obviousness analysis was based on what the combined teachings of the references would have suggested to the POSITA, not bodily incorporation. Specifically, Dr. Alpert explains that the combined teachings would have suggested to the POSITA that Nienaber's delay circuits could be made to be "programmable" in a manner similar to that disclosed in Young. (Appx677.) Dr. Alpert further notes that "[t]his could provide an advantage, for example, of allowing the pads to be bonded according to characterization of the design or testing of a manufactured device." (*Id*.) Neither the Board nor Xilinx relied on a bodily incorporation theory.

II. THE BOARD DID NOT VIOLATE THE ADMINISTRATIVE PROCEDURES ACT

Because PLL's substantive arguments lack merit, it attempts to salvage its claims by arguing that the Board committed procedural errors. But the Board followed the procedures mandated by the AIA and its implementing regulations to the letter. Moreover, PLL failed to take advantage of various procedural

mechanisms available to address the concerns it now raises on appeal. The Board fully complied with the APA.

A. The Board Complied with the APA in Considering Xilinx's Reply.

PLL argues that the Board violated the APA by relying on improper new evidence and arguments in Xilinx's Reply without affording PLL an opportunity to respond. (BlueBr. 45-56.) PLL is wrong. First, PLL waived any argument that the scope of the Reply was improper by failing to raise that issue before the Board. Second, the scope of Xilinx's Reply was proper in any event because it consisted entirely of arguments and evidence narrowly tailored to respond to arguments raised in PLL's Patent Owner Response. Third, PLL had ample opportunity to respond even if Xilinx's Reply exceeded its proper scope.

1. PLL Waived Any Argument that the Scope of Xilinx's Reply was Improper.

The Board provides a variety of procedures for a patent owner to challenge the scope of a petitioner's reply, including conference calls with the Board and oral argument. *See*, *e.g.*, *Corning Inc. v. DSM IP Assets B.V.*, IPR2013-00047, 2014 WL 1783279, at *4 n.3 (PTAB May 1, 2014). There is no record that PLL availed itself of these procedures: PLL did not raise this theory at oral argument or in any of its filed papers, nor is there any record of a conference call initiated for this purpose. Predictably, the Final Written Decision does not discuss this issue. PLL waived its challenge to the scope of Xilinx's Reply by failing to establish that it

raised the issue before the Board, and thus the Court should decline to consider the argument on appeal. *See Software Rights Archive, LLC v. Facebook, Inc.*, --- F. App'x ----, 2016 WL 4709878, at *11 (Fed. Cir. Sept. 9, 2016) (citing cases).

2. The Scope of Xilinx's Reply was Proper.

PLL's challenge would fail even if it had been preserved. PLL's objections are directed to Xilinx's arguments and evidence regarding the construction of the term "clock." (BlueBr. 45-56.) But new arguments and evidence in a reply are permissible under the Board's procedures so long as they are directed to rebutting the patent owner's response. *See*, *e.g.*, *Volkswagen Group of America, Inc. v. Emerachem Holdings, LLC*, IPR2014-01555, 2015 WL 5898727 (PTAB Oct. 9, 2015) (evidence "properly relied upon in a reply" includes that "limited to responding to arguments made in an opposition").

Intelligent Bio-Systems, Inc. v. Illumina Cambridge Ltd., 821 F.3d 1359 (Fed. Cir. 2016), cited by PLL, is inapposite. In that case, the Court held that a petitioner's reply was improper because it presented a new ground of invalidity that was not asserted in the petition. *Id.* at 1369 ("But IBS chose which grounds of invalidity to assert in its petition and it chose not to assert this new one."). The Court also found the Reply to be improper because it "relied on an entirely new rationale" to support the new ground of invalidity. *Id.* at 1369-70.

In the present case, Xilinx did not modify its proposed ground of invalidity in the Reply—it continued to assert that the claims of the '122 patent were obvious over the combination of Nienaber and Young, just as it argued in the Petition. Nor did Xilinx present new rationales in support of the obviousness argument. Rather, all evidence and arguments included in the Reply were directed to rebutting the arguments in PLL's Patent Owner Response. (*See supra* Statement of the Case, Part C.5.) Xilinx's rebuttal evidence and arguments were proper under the Board's procedures. *Volkswagen*, 2015 WL 5898727; *see also* 37 C.F.R. § 42.23(b) (a reply "may respond to arguments raised in the corresponding opposition or patent owner response").

3. PLL Had Multiple Opportunities to Respond to the Evidence and Arguments in Xilinx's Reply.

The thrust of PLL's challenge is that it was unable to respond to the Reply. (BlueBr. 48-55.) But as recognized by this Court, a patent owner in PLL's position "can respond in multiple ways," including by cross-examining an expert, moving to file observations on the cross-examination, moving to exclude or strike, disputing the substance of a reply declaration at oral argument, moving for permission to submit a surreply, and requesting the Board to waive or suspend any regulation that the patent owner believes impairs its ability to respond. *Belden*, 805 F.3d at 1081 (noting that these "options are not mutually exclusive"). These procedures provided PLL with ample opportunities to respond to the Reply, many

of which PLL employed. PLL cannot establish a violation of the APA on the record here.

First, Dr. Alpert's second declaration supported the arguments in Xilinx's Reply that rebutted PLL's Patent Owner Response. (*See* Appx884-913.) PLL then deposed Dr. Alpert, and thus had the opportunity to question him about all aspects of his declaration and the related Reply. (Appx1371-1425.) Moreover, PLL filed a transcript of the deposition with the Board as an exhibit, making that transcript part of the record used by the Board in rendering its Final Written Decision.

Second, PLL filed eight pages of observations on the cross-examination of Dr. Alpert, all of which are directed to the arguments and evidence addressed in Xilinx's Reply. (Appx346-355.) Although PLL argues that observations are "non-argumentative" and "must follow a highly constrained format" (BlueBr. 50), PLL included a significant amount of argument in its observations. For example, in its "Observations Regarding Analog Computers," PLL addressed the portions of the IEEE Dictionary cited by Xilinx in rebuttal, contending that Dr. Alpert's "testimony is relevant because it shows, *contrary to the Petitioner's assertion*, that the IEEE Dictionary's inclusion of terms like 'analog computer' and related terms like 'operational amplifier' (a primary building block of an analog computer) in the 'C' computer category is for merely historical reasons and does not in any way imply that one of ordinary skill in the art would have considered the C category to

include analog concepts and terms generally." (Appx347.) PLL made similar substantive arguments throughout its observations.

PLL tries to minimize the utility of the observations by arguing that the Board "ignored" them (BlueBr. 49), but there is no evidence to support this argument. Rather, the Board repeatedly stated that its Final Written Decision was based on the "full record" developed during trial. (*E.g.*, Appx24-25.) Further, although the Final Written Decision did not mention the observations by name, the decision addressed the substance of many of them. (*See*, *e.g.*, Appx10-12 (addressing the IEEE Dictionary's definition of "clock," as discussed in various observations); Appx25-28 (addressing whether Nienaber discloses a "clock," as discussed in various observations).)

Moreover, the Board was not required to explicitly address each of PLL's observations in its Final Written Decision. The Board's obligation is to articulate "logical and rational" reasons for its decisions, not to "address every argument raised by a party or explain every possible reason supporting its conclusion." *Synopsys, Inc. v. Mentor Graphics Corp.*, 814 F.3d 1309, 1322 (Fed. Cir. 2016). Here, the Board's lengthy, detailed discussion on the proper construction of clock (Appx6-12) easily satisfied its obligation.

Third, the oral hearing before the Board (Appx379-434) provided PLL with an opportunity to respond to Xilinx's Reply. PLL took full advantage of this

opportunity, presenting argument on a variety of topics including the "C" category code of the IEEE Dictionary (Appx413-416) and the patents cited by Xilinx for their disclosure of "analog clock signals" (Appx416-418).

Fourth, if PLL had wanted the Board to disregard the evidence cited in Xilinx's Reply, it could have moved to exclude. *See Genzyme*, 825 F.3d at 1368 (noting that "despite having actual notice that Biomarin was relying on the *in vivo* references to rebut Genzyme's arguments, Genzyme failed to take advantage of its procedural options to seek to exclude that evidence"). PLL declined to pursue this option despite having full notice of Xilinx's evidence in its Reply. Similarly, if PLL had wanted the Board to disregard arguments in Xilinx's Reply, it could have filed a motion to strike. It did not.

Fifth, PLL did not "request that the Board waive or suspend a regulation that the patent owner believes impairs its opportunity to respond to the declaration." *Belden*, 805 F.3d at 1081; *see also* 37 C.F.R. § 42.5(b) ("The Board may waive or suspend a requirement … and may place conditions on the waiver or suspension."). Although PLL complains at length about the inadequacy of the procedures available to it for addressing the Reply (BlueBr. 45-56), it nevertheless failed to request that the Board waive or suspend any regulations.

Sixth, although PLL states that, on a conference call, the Board orally denied it permission to file a surreply, there is nothing in the record to evidence PLL's

request, let alone the Board's denial or the rationale for such denial. The Board has described the proper procedure for using a court reporter on conference calls (*see*, *e.g.*, *Amkor Tech., Inc. v. Tessera, Inc.*, IPR2013-00242, 2013 WL 8701669 (PTAB Nov. 19, 2013)), but PLL apparently declined to retain a court reporter here. *Cf. Redline Detection, LLC v. Star Envirotech, Inc.*, IPR2013-00106, 2013 WL 5970198, at *6 (PTAB Sept. 11, 2013) (emphasizing that "Patent Owner provided a court reporter and arranged for the preparation of a transcript of the initial conference and for the timely inclusion of that transcript in the record of this trial"). Having failed to obtain a transcript, PLL is not permitted to rely on its subjective recollection. *See*, *e.g.*, *Gonzales v. Def. Logistics Agency*, 772 F.2d 887, 890-91 (Fed. Cir. 1985) ("if petitioner wishes to rely on any part of the record of the hearing he is required to provide it"). To allow PLL to rely on a conference call that is not reflected in the record would prejudice Xilinx, which cannot address the details of the call without further improper supplementation of the record.

Finally, this case is easily distinguishable from *NuVasive*, in which this Court recently found an APA violation when the Board failed to provide an opportunity for a patent owner to address a portion of a prior art reference cited for the first time in a petitioner's reply. 2016 WL 6608999, at *3, *5-6. In *NuVasive*, not only did the record reflect that the Board denied the patent owner's request for leave to file a motion to strike or a surreply, but the Board refused to allow the

patent owner to address the newly-cited portion of the prior art reference at oral argument. *Id.* at *3. Neither circumstance is present here. Further, the arguments and evidence in Xilinx's Reply were directed solely to rebutting arguments and evidence first raised in PLL's Patent Owner Response, and they did not raise a new obviousness rationale. PLL had multiple opportunities to address the arguments and evidence, many of which PLL took advantage of, and others that it forfeited.

In short, even a denial of leave to file a surreply—the only evidentiary ruling that PLL alleges restricted its ability to respond here—would not establish an APA violation under the circumstances of this case, particularly absent any record establishing the context of the request and denial. *See Belden*, 805 F.3d at 1082 ("Where new enough matter is allowed on rebuttal, surrebuttal may be allowed, *but a proffer of specifics may be required* to justify the additional round of evidentiary submissions."). PLL's claim of procedural error lacks merit.

B. The Board's Final Written Decision Did Not Rely on "New Rationales" in Violation of the APA.

In its Final Written Decision, the Board correctly found that the POSITA would be motivated to combine Nienaber and Young. (Appx28-33.) In making that determination, the Board provided the following rationales, among others:

> (i) an obviousness analysis must take into account the modifications that the POSITA would make to a prior art reference, and here, "it was well within the level of skill … in this art to make any modifications necessary" (Appx30-31);

> (ii) the '122 patent describes "programmable delay circuits" as being "conventional," and this admitted prior art evidences the knowledge that the POSITA would bring to bear in reading the prior art (Appx31); and
>
> (iii) the POSITA would have been motivated to "update[] those analog components [of Nienaber] using more modern digital components, as taught in Young" (*id.*).

PLL mistakenly argues that the Board's reliance on the above rationales violates the APA. (BlueBr. 69-73.) In fact, PLL had notice of each of the alleged "new rationales" and an opportunity to respond to them. Nothing more is required by the APA. *See Belden*, 805 F.3d at 1080.

First, PLL argues that the Final Written Decision's reliance on the admitted prior art of the '122 patent was an improper new rationale for which PLL was not given notice. (BlueBr. 70-71.) This is false. Xilinx's Petition described the admitted prior art and included a discussion of why this admitted prior art tended to show the unpatentability of the claims. (Appx60-63.) Accordingly, PLL had notice of this rationale and opportunities to address it in any of its papers and at oral argument. In fact, PLL did address it at oral argument. (Appx426-428.)

Further, this Court has stated that the Board may consider art that documents the knowledge the POSITA would bring to bear in reading prior art identified as producing obviousness, even if that art is not one of the pieces of prior art defining the obviousness combination. *Ariosa Diagnostics v. Verinata Health, Inc.*, 805

F.3d 1359, 1365 (Fed. Cir. 2015). That is precisely how the court considered the admitted prior art here. (Appx31.)

Second, PLL argues that "the Board violated the APA when the final written decision supported the obviousness conclusion with the rationale that one of ordinary skill in the art would have updated Nienaber's analog components with digital ones…. PLL had absolutely no notice of that rationale until the Board first mentioned it during the oral argument." (BlueBr. 72.) This, too, is false. In its Institution Decision, the Board used this rationale in explaining why the POSITA would be motivated to combine Nienaber and Young. (Appx196 ("Indeed, often it can be routine to use digital components to upgrade existing analog devices.").) Thus, PLL had notice of this argument as early as the Institution Decision and could have responded to it at least in its Patent Owner Response and at oral argument. In fact, Xilinx raised this rationale at oral argument (Appx395-396), and PLL responded to it (Appx425). PLL's objection on this ground is flatly contradicted by the record.

Third, PLL argues that the Final Written Decision's reliance on the assertion that the POSITA would have made "any modification necessary" was an improper new rationale for which PLL was not given notice. (BlueBr. 70-71.) PLL's argument is based on the erroneous premise that Xilinx proposed substituting Young's delay line 27 into Nienaber *without modification*. But as explained above

(*see supra* Part I.C.2), Xilinx never proposed a "bodily incorporation" theory. The Board's statement that the POSITA could make modifications to the references, as necessary, is consistent with Xilinx's argument throughout the proceeding and rests on fundamental obviousness principles. *See In re ICON Health & Fitness, Inc.*, 496 F.3d 1374, 1382 (Fed. Cir. 2007) ("[W]e do not ignore the modifications that one skilled in the art would make to a device borrowed from the prior art.").

Finally, assuming *arguendo* that the Board relied on "new rationales" in violation of the APA, any such error was harmless. As discussed above (*see supra* Statement of the Case, Part C.7), the Board identified several independent reasons for its finding that the POSITA would be motivated to combine Nienaber and Young. (*See* Appx28-33.) Thus, even if the allegedly "new" rationales are disregarded, the Board's decision is supported by substantial evidence. *See Progressive Cas. Ins. Co. v. Liberty Mut. Ins. Co.*, 625 F. App'x 552, 557 (Fed. Cir. 2015).

CONCLUSION

Xilinx respectfully requests that the Court affirm the Board's determinations that claims 1-10, 12-14, and 16-20 of the '122 patent are unpatentable.

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Respectfully submitted,

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CERTIFICATE OF COMPLIANCE

1. This brief complies with the type-volume limitation of Federal Rule of Appellate Procedure 32(a)(7)(B) because the brief contains 13,711 words, excluding the parts of the brief exempted by Federal Rule of Appellate Procedure 32(a)(7)(B)(iii) and Federal Circuit Rule 32(b).

2. This brief complies with the typeface requirements of Federal Rule of Appellate Procedure 32(a)(5) and the type style requirements of Federal Rule of Appellate Procedure 32(a)(6). The brief has been prepared in a proportionally spaced typeface using Microsoft Word 2007 in 14-point Times New Roman font.

Dated: December 5, 2016

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CERTIFICATE OF SERVICE

I hereby certify that on December 5, 2016, I caused the foregoing brief to be filed via CM/ECF with the Clerk of the Court, thereby electronically serving it on all counsel of record in this matter.

Dated: December 5, 2016

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